WHAT IS CLAIMED IS:

1. A thin film transistor array substrate, comprising:

a gate pattern including:

a gate electrode of the thin film transistor;

a gate line to which the gate electrode is connected; and

a gate pad to which the gate line is connected;

a source/drain pattern including:

a source electrode and a drain electrode of the thin film transistor;

a data line connected to the source electrode;

a data pad connected to the data line;

a storage electrode formed and superimposed with the gate line;

a semiconductor pattern formed in a low region of the substrate corresponding to the source/drain pattern;

a transparent electrode including a pixel electrode connected to the drain electrode and the storage electrode, a gate pad protection electrode covering the gate pad, and a data pad protection electrode formed to cover the data pad; and

a protection pattern and a gate insulation pattern stacked in the remainder region except for the region where the transparent electrode pattern is formed.

2. The thin film transistor array substrate according to claim 1, wherein the protection pattern partially exposes the drain electrode and the storage electrode and is connected to the pixel electrode.

3. A method of manufacturing a thin film transistor array substrate, comprising:

forming using a first mask process, a gate electrode of the thin film transistor on the substrate, a gate line connected to the gate electrode, a gate pattern including the gate pad connected to the gate line;

forming a gate insulation film on the substrate where the gate pattern is formed;

forming using a second mask process a source electrode and a drain electrode of the

thin film transistor on the gate insulation film, a data line connected to the source electrode, a data pad connected to the data line, a source/drain pattern including a storage electrode in the region superimposed with the gate line, and a semiconductor pattern formed corresponding to the source/drain pattern on the low part; and

forming using a third mask process a pixel electrode connected to the drain electrode and the storage electrode, a gate pad protection electrode formed to cover the gate pad, a transparent electrode pattern including the data pad protection electrode formed to cover the data pad, and a gate insulation pattern and a protection film pattern stacked in the a region other than the region where the transparent electrode pattern is formed.

4. The method of manufacturing the thin film transistor array substrate according to claim 3, wherein the second mask process uses a diffraction exposure mask having the diffraction exposure part in the channel part of the thin film transistor.

5. The method of manufacturing the thin film transistor array substrate according to claim 3, wherein the second mask process comprises:

sequentially forming a semiconductor layer, and a source/drain metal layer on the gate insulation film;

forming by use of the diffraction exposure mask a photoresist pattern where the channel part of the thin film transistor has a height lower than the source/drain pattern part;

patterning the source/drain metal layer and the semiconductor layer by use of the photoresist pattern;

ashing the photoresist pattern to a prescribed depth;

removing a source/drain metal layer of the channel part of the thin film transistor by use of the ashed photoresist pattern; and

removing the photoresist pattern by a strip process.

6. The method of manufacturing the thin film transistor array substrate according to claim 3, wherein the third mask process comprises:

forming a protection film on the substrate where source/drain pattern is formed;

forming the photoresist pattern using the third mask;

forming the gate insulation pattern and the protection film pattern using the protection film pattern and the insulation film using the photoresist pattern;

evaporating a transparent electrode material on the substrate where the photoresist pattern exists; and

forming the transparent electrode pattern by removing the photoresist pattern by strip process and the transparent electrode material.

7. The method of manufacturing the thin film transistor array substrate according to claim 3, wherein the protection film pattern partially exposes the drain electrode and the storage electrode and is connected to the pixel electrode.

8. A thin film transistor array substrate, comprising:

a gate electrode of the thin film transistor;

a gate line to which the gate electrode is connected; and

a gate pad to which the gate line is connected;

a source electrode and a drain electrode of the thin film transistor;

a data line connected to the source electrode;

a data pad connected to the data line;

a storage electrode formed and superimposed over the gate line;

a transparent electrode including a pixel electrode connected to the drain electrode and the storage electrode, a gate pad protection electrode covering the gate pad, and a data pad protection electrode formed to cover the data pad; and

a protection layer and a gate insulation layer stacked in a region of the substrate other than the region where the transparent electrode is formed.

9. The thin film transistor array substrate according to claim 8, wherein the protection layer partially exposes the drain electrode and the storage electrode and is connected to the pixel electrode.

10. A method of manufacturing a thin film transistor array substrate, comprising:

forming using a first mask process, a gate electrode of the thin film transistor on the substrate, a gate line connected to the gate electrode, and a gate pad connected to the gate line;

forming a gate insulation film on the substrate where the gate pad is formed;

forming using a second mask process a source electrode and a drain electrode of the thin film transistor on the gate insulation film, a data line connected to the source electrode, a data pad connected to the data line, a storage electrode superimposed over the gate line; and

forming a pixel electrode using a third mask process connected to the drain electrode and the storage electrode, a gate pad protection electrode formed to cover the gate pad, a transparent electrode, a data pad protection electrode covering the data pad, and a gate insulation pattern and a protection-film pattern stacked in the a region other than the region where the transparent electrode is formed.

11. The method of manufacturing the thin film transistor array substrate according to claim 10, wherein the second mask process uses a diffraction exposure mask having the diffraction exposure part in the channel part of the thin film transistor.

12. The method of manufacturing the thin film transistor array substrate according to claim 10, wherein the second mask process comprises:

sequentially forming a semiconductor layer, and a source/drain metal layer on the gate insulation film;

forming by use of the diffraction exposure mask a photoresist pattern where the channel part of the thin film transistor has a height lower than the storage electrode;

patterning the source/drain metal layer and the semiconductor layer using the photoresist;

ashing the photoresist to a prescribed depth;

removing a source/drain metal layer of the channel part of the thin film transistor by use of the ashed photoresist; and

removing the photoresist by a strip process.

13. The method of manufacturing the thin film transistor array substrate according to claim 10, wherein the third mask process comprises:

forming a protection film on the substrate where the storage electrode is formed;

forming the photoresist using the third mask;

forming the gate insulation pattern and the protection film pattern using the protection film pattern and the insulation film using the photoresist;

evaporating a transparent electrode material on the substrate where the photoresist exists; and

forming the transparent electrode pattern by removing the photoresist by strip process and the transparent electrode material.

14. The method of manufacturing the thin film transistor array substrate according to claim 10, wherein the protection film pattern partially exposes the drain electrode and the storage electrode and is connected to the pixel electrode.